Digital Design

CSCE 2114-L007

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November 23, 2016

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Introduction

This lab consisted of writing VHDL code from scratch in order to simulate a rising edge triggered T flip-flop that has an asynchronous active low clear input and an asynchronous active low preset input. Writing all the code from scratch proved to be more difficult than what was originally anticipated since VHDL code isn’t something that is covered very well in class.

Design

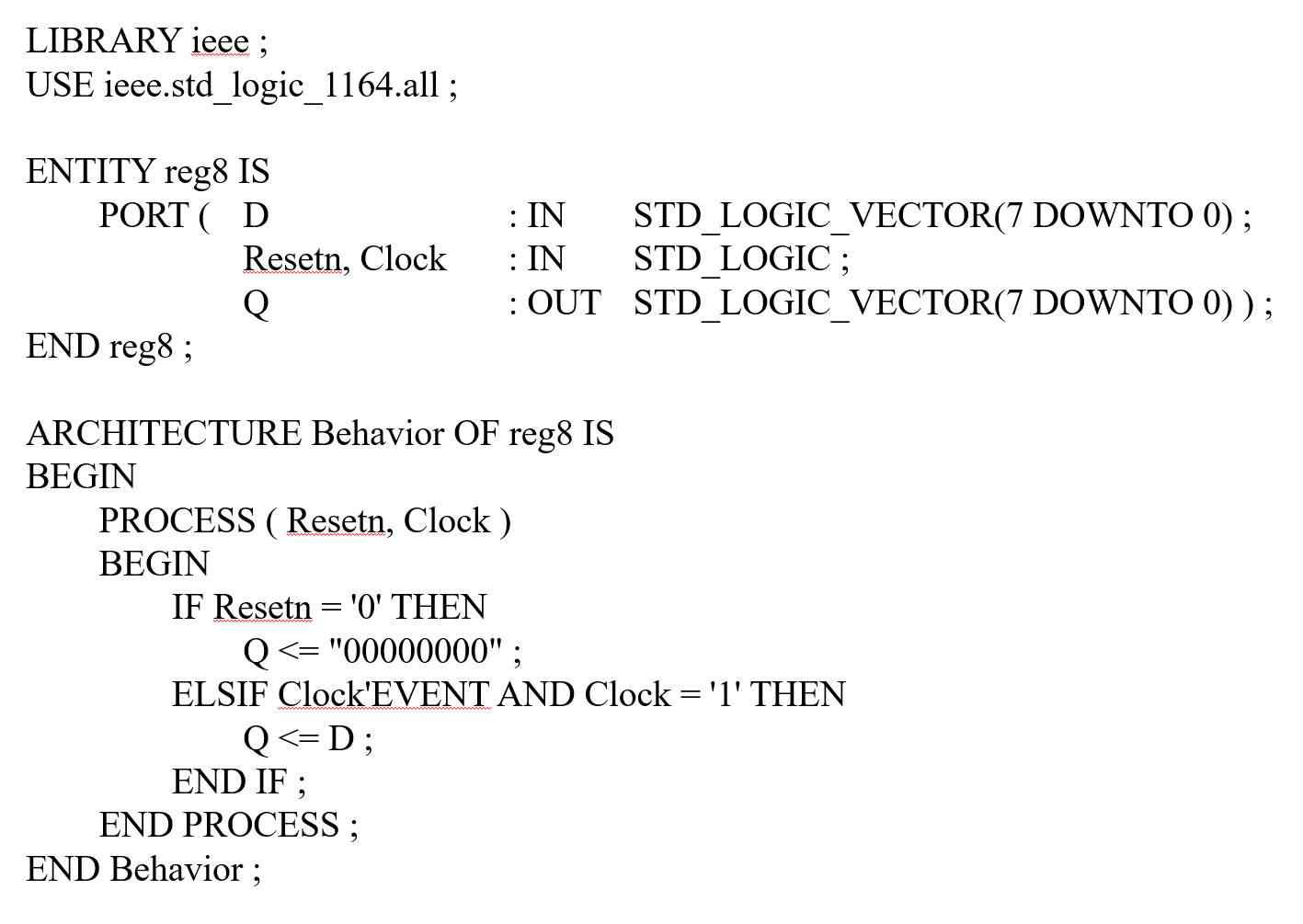
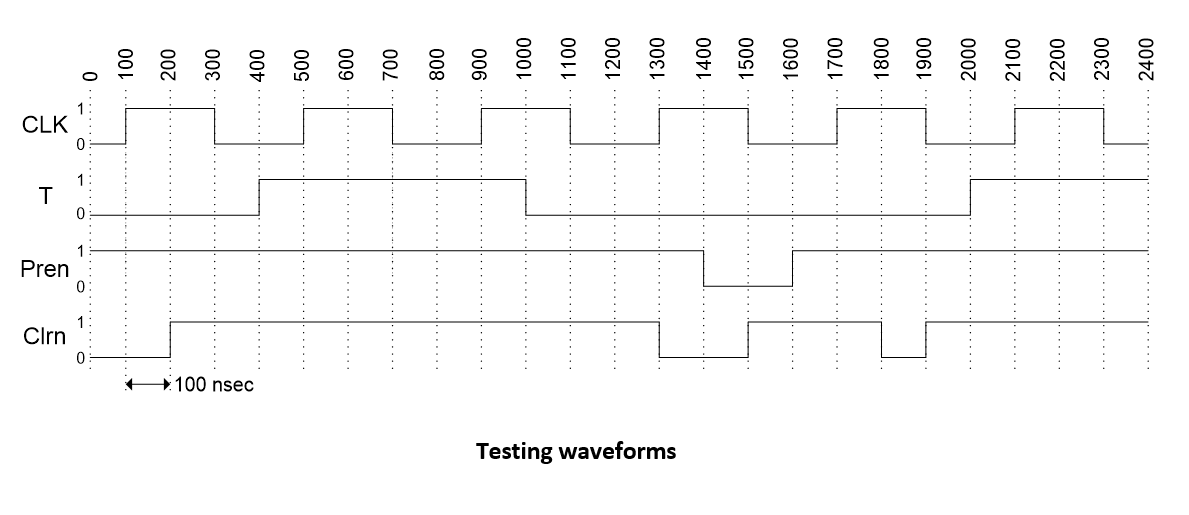
How to start the VHDL code was not hard because there are numerous amounts of powerpoints that have pictures from the textbook of VHDL code. The hard part comes in where if asks you write the process. Unfortunately, the files that had the VHDL code and the vector waveform graph were lost and are unable to be retrieved but the powerpoints have an example of what the code for something like this should look like albeit without having the toggle input or the Qn, Pren, and Clrn outputs. A picture of that code will be shown below. One thing that does come to mind is how Qn was used and how it was made. A temporary variable needed to be used and set equal to Q. Once that was done, everywhere in that Q is equal to something in the code below got replaced with that temporary variable. After the IF statements that temporary variable is then set to Qn. Another thing that comes to mind is that Pren was used in place of Resetn in the code below. 

Figure : VHDL code from the VHDL Notes powerpoint

Results

The results are somewhat of an enigma at this point. The files that had the picture of the vector waveform graph were lost and are unable to be retrieved from the campus computer due to where this computer is located. The only thing that is available is a picture of how the inputs should be implanted into the vector waveform graph. A picture of that will be shown below. If memory serves, the only time Q ever changed on the rising edge of the clock was when Clrn changed from 0 to 1. 

Conclusion

This lab did not seem like it was going to be a very long one but because the VHDL code had to be written from scratch and due to a lack of knowledge of how to write in VHDL it made this lab last a bit longer than what was originally anticipated. The work seems all for naught because the files were lost. If only the file that VHDL code didn’t get lost, then that could have been copied into the free version of Quartus.